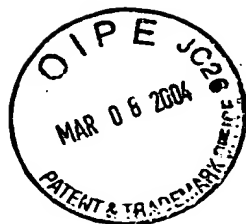


Amendments to the Drawings:

Amendments to the drawings have previously been approved. Applicant files replacement formal drawings incorporating these changes.



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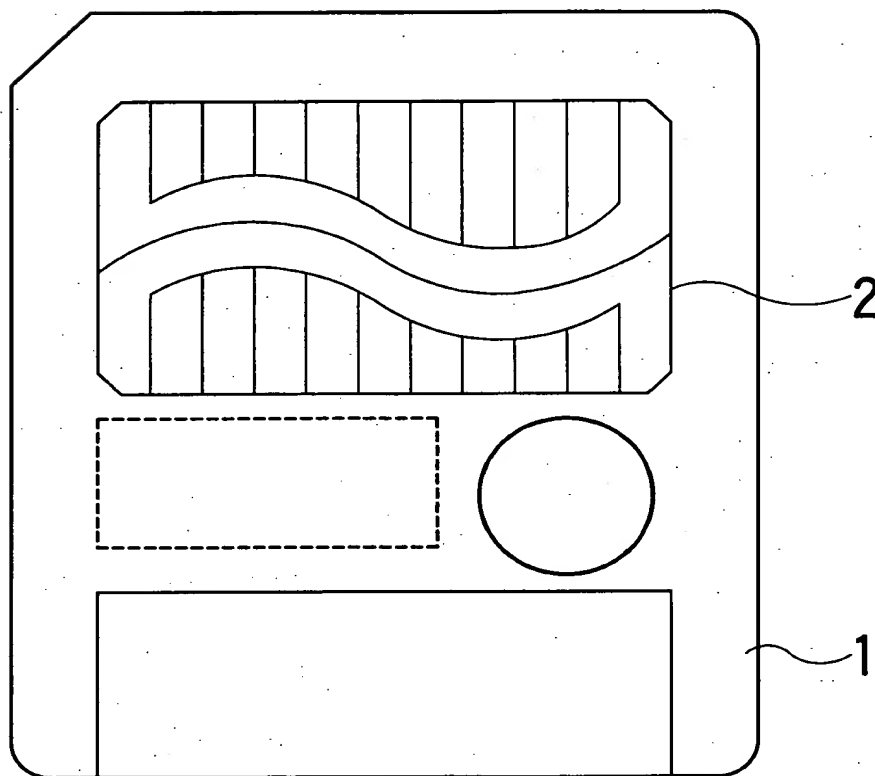


FIG. 1

PRIOR ART



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	0	255	256	263
PHYSICAL BLOCK 0	Page 0	DATA AREA (256BYTES)	REDUNDANT DIVISION (16BYTES)	
	Page 1			
	⋮			
	Page 15			
PHYSICAL BLOCK 1	Page 0			
	Page 1			
	⋮			
	Page 15			
⋮	⋮	⋮	⋮	
PHYSICAL BLOCK 511	Page 0			
	Page 1			
	⋮			
	Page 15		21/45	

FIG. 2

PRIOR ART



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PHYSICAL BLOCK 0	SECTOR 0	512 BYTES
	SECTOR 1	
	⋮	
	SECTOR 7	
PHYSICAL BLOCK 1	SECTOR 8	
	SECTOR 9	
	⋮	
	SECTOR 15	
⋮	⋮	⋮
PHYSICAL BLOCK 499	SECTOR 3992	
	SECTOR 3993	
	⋮	
	SECTOR 3999	

FIG. 3

PRIOR ART



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DATA DIVISION

BYTE	PAGE 0(EVEN PAGE)	PAGE 1(ODD PAGE)
0~255	DATA Area-1	DATA Area-2

REDUNDANT DIVISION

BYTE	EVEN PAGE	ODD PAGE
256	User Data Area	ECC Area-2
257		
258		
259		
260	Data Status Area	Block Address Area-2
261	Block Status Area	
262	Block Address Area-1	ECC Area-1
263		

FIG. 4

PRIOR ART



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		0	511	512	527
PHYSICAL BLOCK 0	Page 0	DATA AREA	REDUNDANT DIVISION (16BYTES)		
	Page 1				
	⋮				
	Page 15				
PHYSICAL BLOCK 1	Page 0				
	Page 1				
	⋮				
	Page 15				
⋮	⋮	⋮	⋮	⋮	⋮
PHYSICAL BLOCK 1023	Page 0				
	Page 1				
	⋮				
	Page 15				

FIG. 5

PRIOR ART



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LOGICAL BLOCK 0	SECTOR 0	512 BYTES
	SECTOR 1	
	⋮	
	SECTOR 15	
LOGICAL BLOCK 1	SECTOR 16	
	SECTOR 17	
	⋮	
	SECTOR 31	
⋮	⋮	⋮
LOGICAL BLOCK 999	SECTOR 15984	
	SECTOR 15985	
	⋮	
	SECTOR 15999	

FIG. 6

PRIOR ART



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DATA DIVISION

BYTE	
0~511	DATA Area

REDUNDANT DIVISION

BYTE	
512	User Data Area
513	
514	
515	
516	Data Status Area
517	Block Status Area
518	Block Address Area-1
519	
520	ECC Area-2
521	
522	
523	Block Address Area-2
524	
525	ECC Area-1
526	
527	

FIG. 7

PRIOR ART



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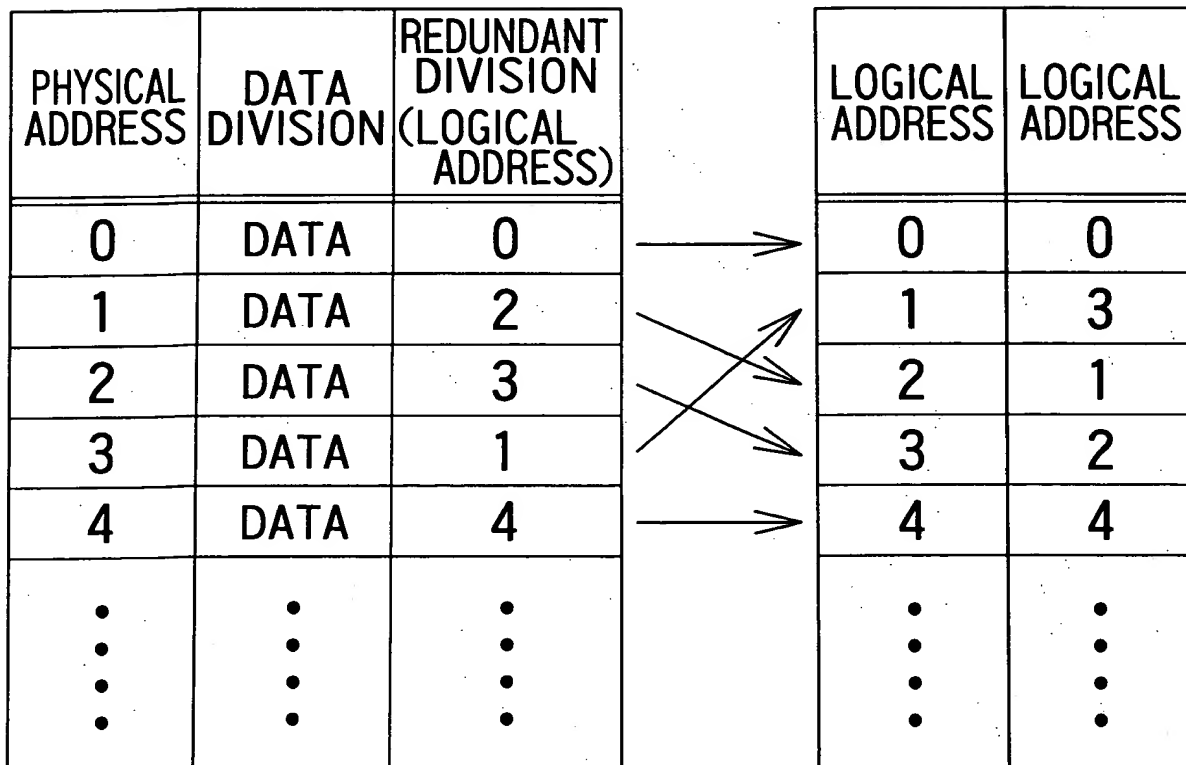


FIG. 8
PRIOR ART



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OFFSET (LOGICAL BLOCK ADDRESS)	PHYSICAL BLOCK ADDRESS	PHYSICAL BLOCK ADDRESS (BINARY DATA)			
		UPPER BYTE		LOWER BYTE	
word0(LBA=0)	0	0000	0000	0000	0000
word1(LBA=1)	500	0000	0001	1111	0100
word2(LBA=2)	327	0000	0001	0100	0111
⋮	⋮	⋮	⋮	⋮	⋮
word497(LBA=497)	244	0000	0000	1111	0100
word498(LBA=498)	249	0000	0001	1110	1111
word499(LBA=499)	128	0000	0001	1000	0000

FIG. 9

PRIOR ART

OFFSET (LOGICAL BLOCK ADDRESS)	PHYSICAL BLOCK ADDRESS	PHYSICAL BLOCK ADDRESS (BINARY DATA)			
		UPPER BYTE		LOWER BYTE	
word0(LBA=0)	0	0000	0000	0000	0000
word1(LBA=1)	1000	0000	0011	1110	1000
word2(LBA=2)	654	0000	0010	1000	1110
⋮	⋮	⋮	⋮	⋮	⋮
word997(LBA=997)	488	0000	0001	1110	1000
word998(LBA=998)	498	0000	0001	1111	0010
word999(LBA=999)	256	0000	0001	0000	0000

FIG. 10

PRIOR ART



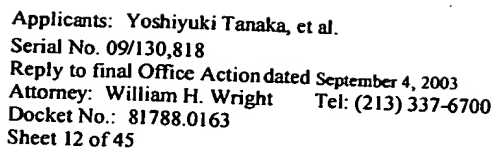
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D7	D6	D5	D4	D3	D2	D1	D0	256 + 8 BYTE/PAGE
0	0	0	1	BA10	BA9	BA8	BA7	262 BYTE(EVEN PAGE) 259 BYTE(ODD PAGE)
BA6	BA5	BA4	BA3	BA2	BA1	BA0	P	263 BYTE(EVEN PAGE) 260 BYTE(ODD PAGE)

BA10~BA0: LOGICAL BLOCK ADDRESS
P EVEN PARITY BIT "1" FIXED VALUE

FIG. 11

PRIOR ART



The diagram illustrates the garbage collection process in a NAND flash memory, showing the state of four NAND blocks (A, B, C, D) and four clusters (A, B, C, D) across four stages of the process.

Logical Address and Physical Block: The diagram is organized into columns for Logical Address (32-63) and Physical Block (A, B, C, D). The Physical Block column is divided into four sections, each representing a NAND block. Each section contains a vertical list of logical addresses (32-63) and a corresponding physical block label (A, B, C, D).

Cluster A Update: A "CLUSTER UPDATE" operation is shown on the left, indicating that data from Cluster A is being updated. This is represented by a shaded box labeled "CLUSTER A" with an arrow pointing to the logical address 48 in the Physical Block A section.

Garbage Collection Process:

- Stage 1:** Data from Cluster A (logical addresses 32-47) is copied to Cluster A' (logical addresses 48-63) in Physical Block A. Cluster B (logical addresses 48-63) is also copied to Cluster B' (logical addresses 48-63) in Physical Block B. Cluster C (logical addresses 48-63) is copied to Cluster C' (logical addresses 48-63) in Physical Block C. Cluster D (logical addresses 48-63) is copied to Cluster D' (logical addresses 48-63) in Physical Block D.
- Stage 2:** The data from Cluster A' (logical addresses 48-63) is copied to Cluster A'' (logical addresses 48-63) in Physical Block A. Cluster B' (logical addresses 48-63) is copied to Cluster B'' (logical addresses 48-63) in Physical Block B. Cluster C' (logical addresses 48-63) is copied to Cluster C'' (logical addresses 48-63) in Physical Block C. Cluster D' (logical addresses 48-63) is copied to Cluster D'' (logical addresses 48-63) in Physical Block D.
- Stage 3:** The data from Cluster A'' (logical addresses 48-63) is copied to Cluster A''' (logical addresses 48-63) in Physical Block A. Cluster B'' (logical addresses 48-63) is copied to Cluster B''' (logical addresses 48-63) in Physical Block B. Cluster C'' (logical addresses 48-63) is copied to Cluster C''' (logical addresses 48-63) in Physical Block C. Cluster D'' (logical addresses 48-63) is copied to Cluster D''' (logical addresses 48-63) in Physical Block D.
- Stage 4:** The data from Cluster A''' (logical addresses 48-63) is copied to Cluster A'''' (logical addresses 48-63) in Physical Block A. Cluster B''' (logical addresses 48-63) is copied to Cluster B'''' (logical addresses 48-63) in Physical Block B. Cluster C''' (logical addresses 48-63) is copied to Cluster C'''' (logical addresses 48-63) in Physical Block C. Cluster D''' (logical addresses 48-63) is copied to Cluster D'''' (logical addresses 48-63) in Physical Block D.

Final State: The final state shows that the data from the old clusters (A, B, C, D) has been successfully moved to the new clusters (A', B', C', D'). The old clusters (A, B, C, D) are now empty, and the new clusters (A', B', C', D') contain the updated data. The logical addresses 32-47 are now empty in all physical blocks, and the logical addresses 48-63 are now occupied by the updated data in the new clusters.

FIG. 13
PRIOR ART



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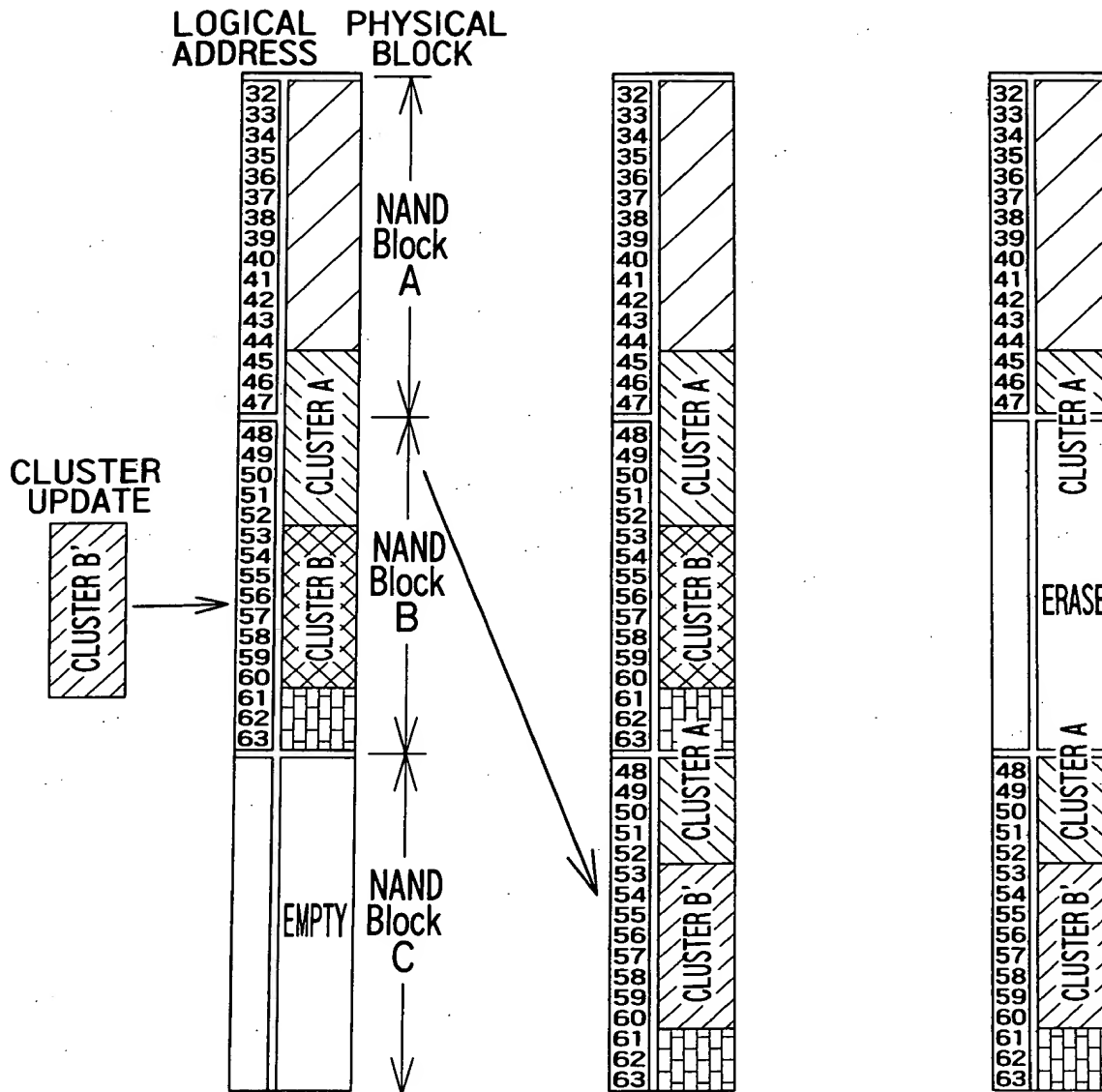


FIG. 14

PRIOR ART



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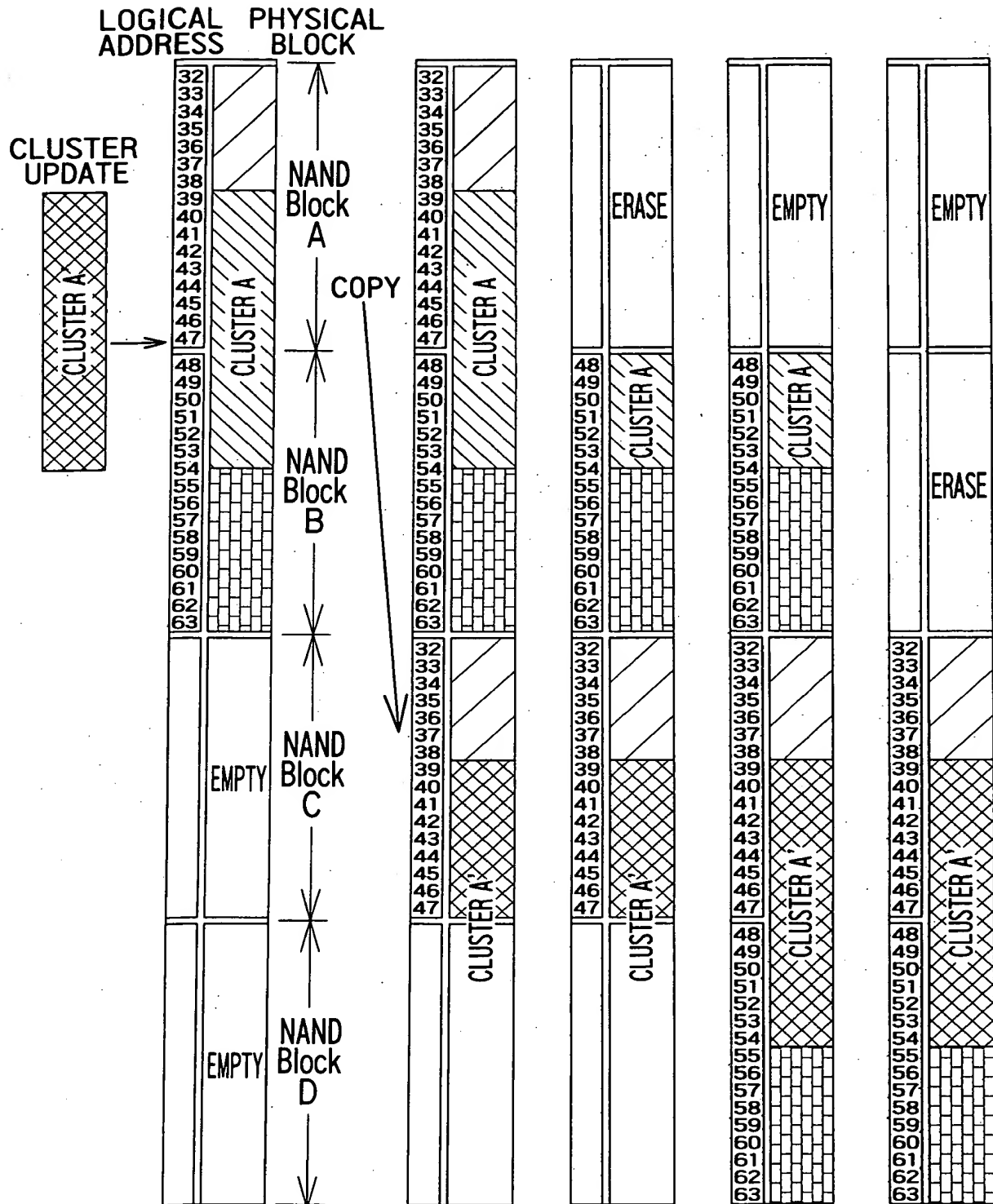


FIG. 15
PRIOR ART



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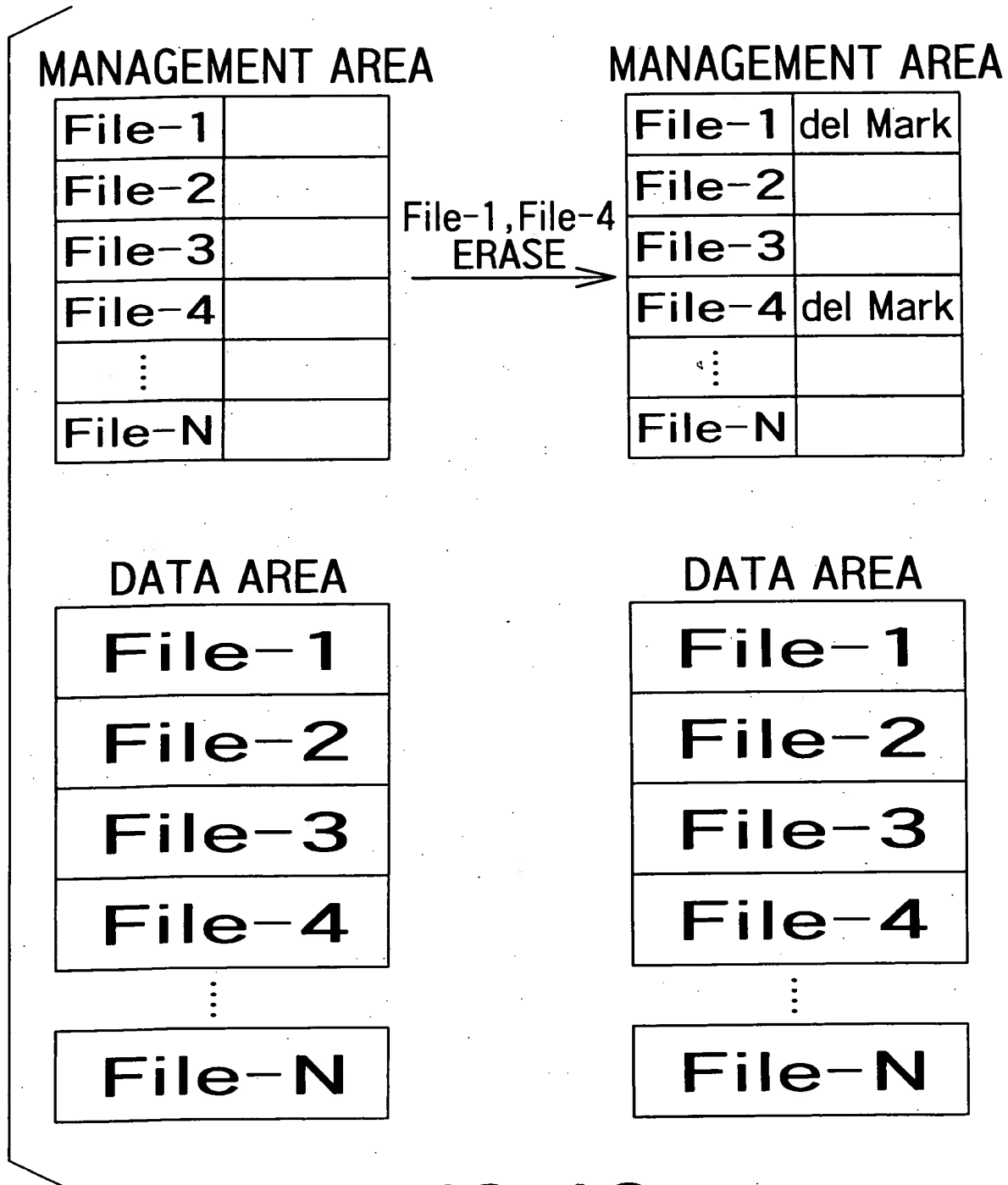


FIG. 16
PRIOR ART



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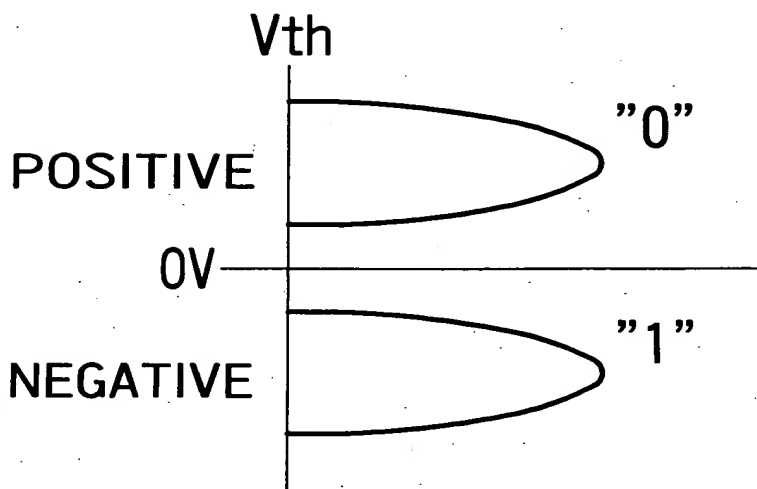


FIG. 17
PRIOR ART

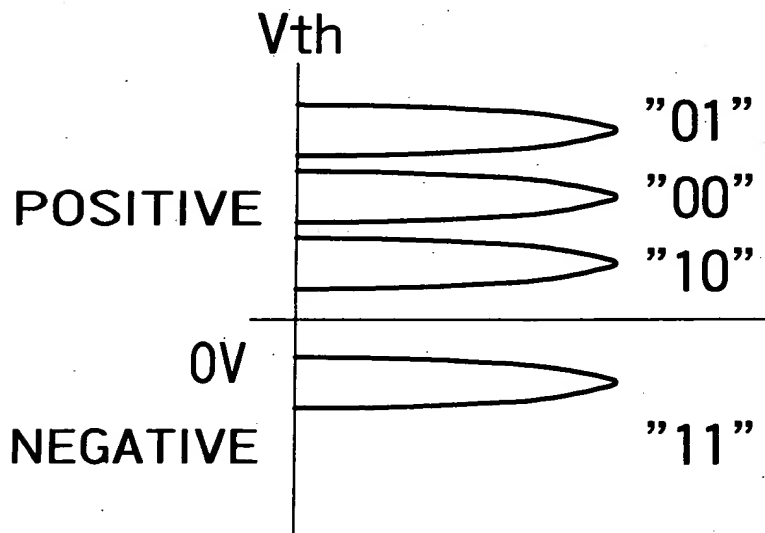


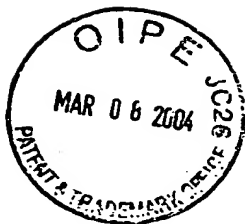
FIG. 18
PRIOR ART



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CARD IN FIG. 2(a)	CARD IN FIG. 2(b)
<div><div>CPU</div><div>ECC CIRCUIT 1</div></div> <div>SYSTEM A</div>	VNAVAILABLE
VNAVAILABLE	AVAILABLE

FIG. 19
PRIOR ART



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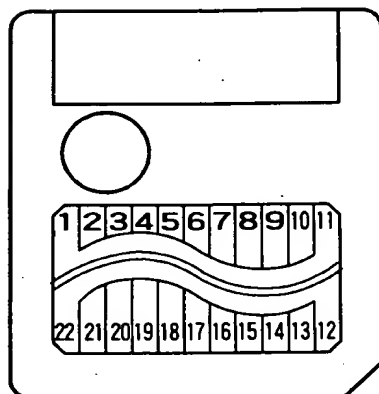


FIG. 20

1,10,11	V _{SS}	POWER SUPPLY (GND)
2	CLE	COMMAND LATCH ENABLE
3	ALE	ADDRESS LATCH ENABLE
4	\overline{WE}	WRITE ENABLE
5	\overline{WP}	WRITE PROTECT
6-9	I/O ₁₋₄	ADDRESS DATA COMMAND INPUT-OUTPUT PORT
13-16	I/O ₅₋₈	ADDRESS DATA COMMAND INPUT-OUTPUT PORT
17	NC	N_C
18	GND	GND LEVEL INPUT
19	R/ \overline{B}	READY BUSY OUTPUT
20	\overline{RE}	READ ENABLE
21	\overline{CE}	CHIP ENABLE
22,23	V _{CC}	POWER SUPPLY

FIG. 21



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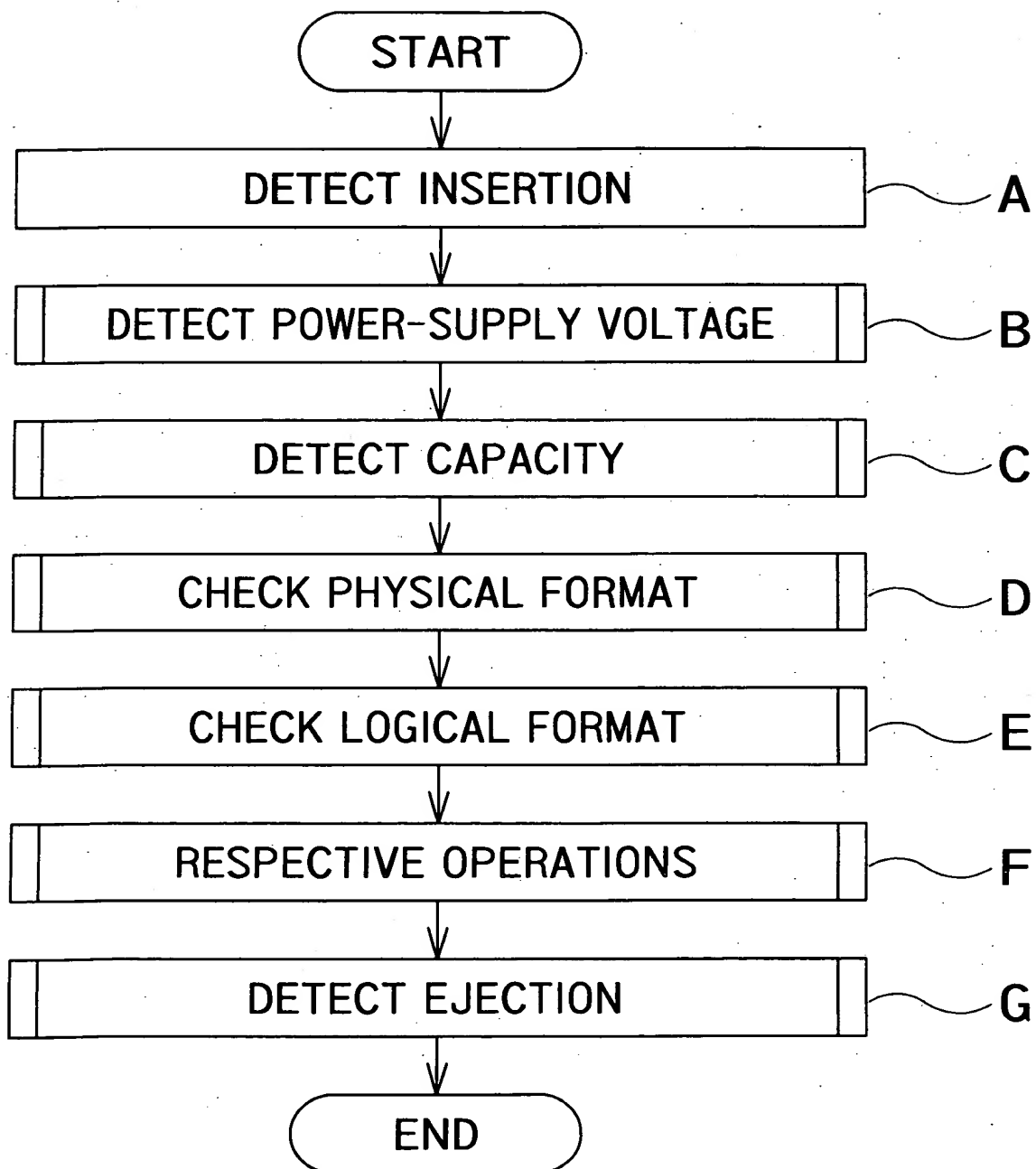
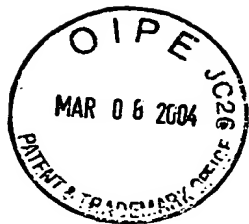
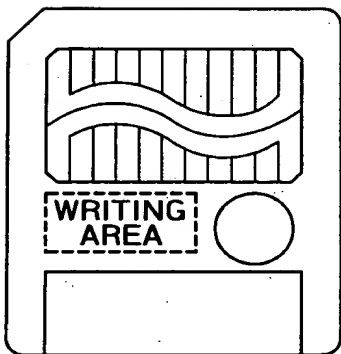


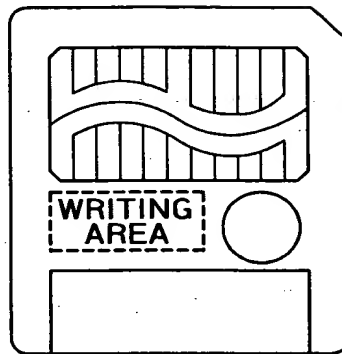
FIG. 22



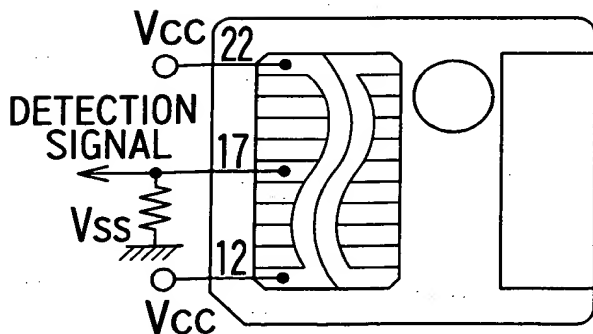
20/45



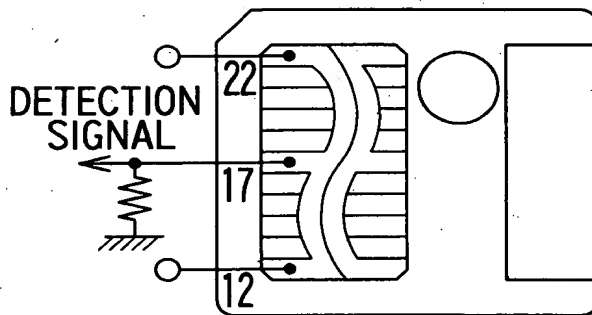
5V PRODUCT
FIG. 23(a)



3.3V PRODUCT
FIG. 23(b)



5V PRODUCT
FIG. 24(a)



3.3V PRODUCT
FIG. 24(b)



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5V DEDICATED CONNECTOR

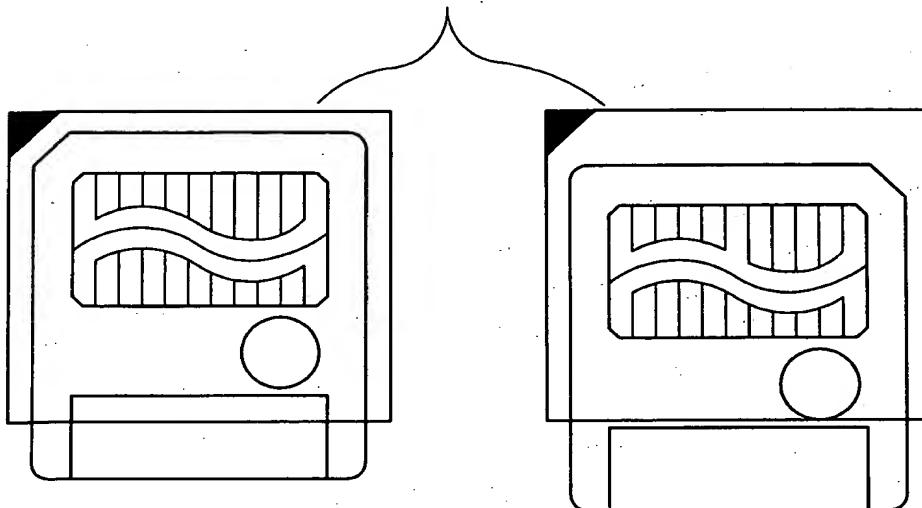


FIG. 25

3.3V DEDICATED CONNECTOR

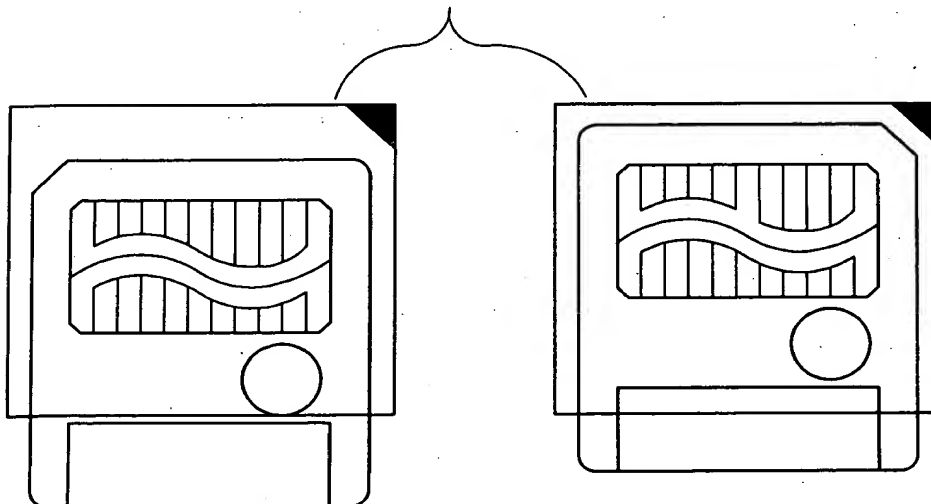


FIG. 26



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5V/3.3V DEDICATED CONNECTOR

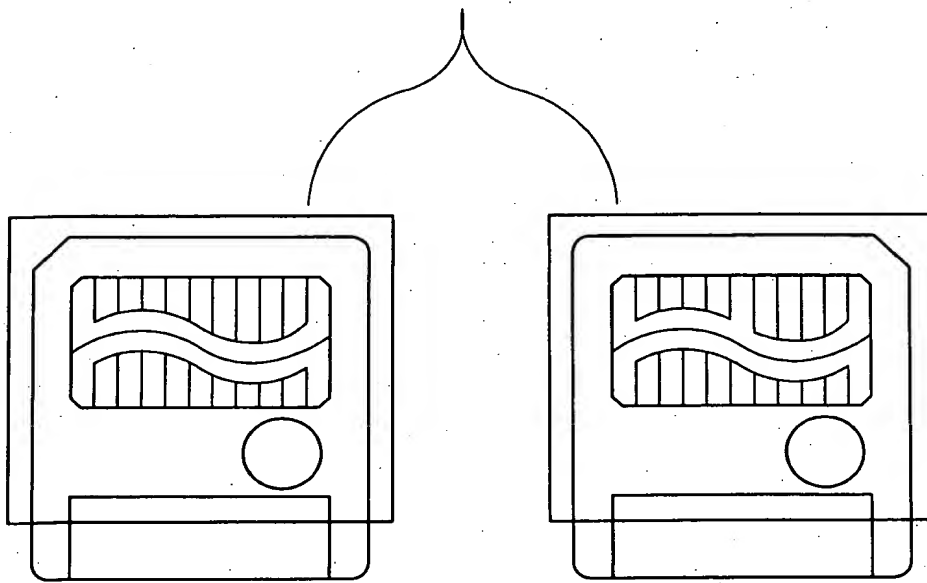


FIG. 27



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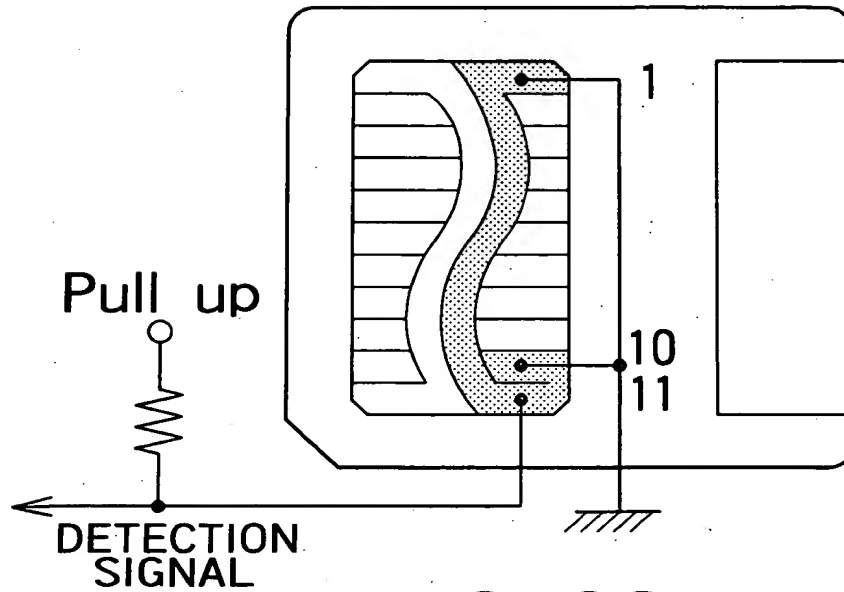


FIG. 28

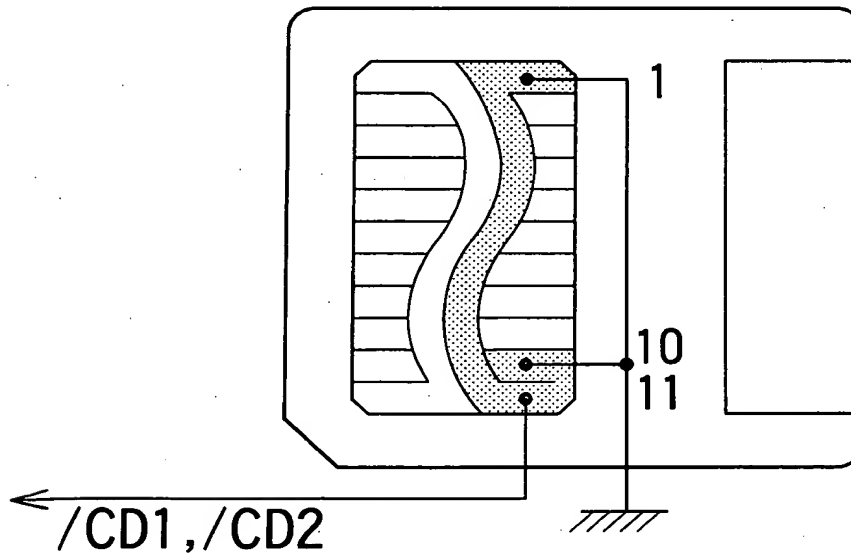


FIG. 29



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bit7	bit6		bit1			bit0	
1stByte	00000000 111		00000000 110			00000000 001	00000000 000
2ndByte	00000000 111		00000001 110			00000001 001	00000001 000
:	:		:	:	:	:	:
255thByte	11111110 111		11111110 110			11111110 001	11111110 000
266thByte	11111111 111		11111111 110			11111111 001	11111111 000

FIG. 30

LP00=D(*****0、***) 、 LP01=D(*****1、***)
 LP02=D(*****0*、***) 、 LP03=D(*****1*、***)
 LP04=D(*****0**、***) 、 LP05=D(*****1**、***)
 LP06=D(****0***、***) 、 LP07=D(****1***、***)
 LP08=D(**0****、***) 、 LP09=D(**1****、***)
 LP010=D(**0****、***) 、 LP011=D(**1****、***)
 LP012=D(*0****、***) 、 LP013=D(*1****、***)
 LP014=D(0****、***) 、 LP015=D(1****、***)
 LP00=D(*****,**0) 、 LP01=D(*****,**1)
 LP02=D(*****,*0*) 、 LP03=D(*****,*1*)
 LP04=D(*****,0**) 、 LP05=D(*****,1**)

FIG. 31

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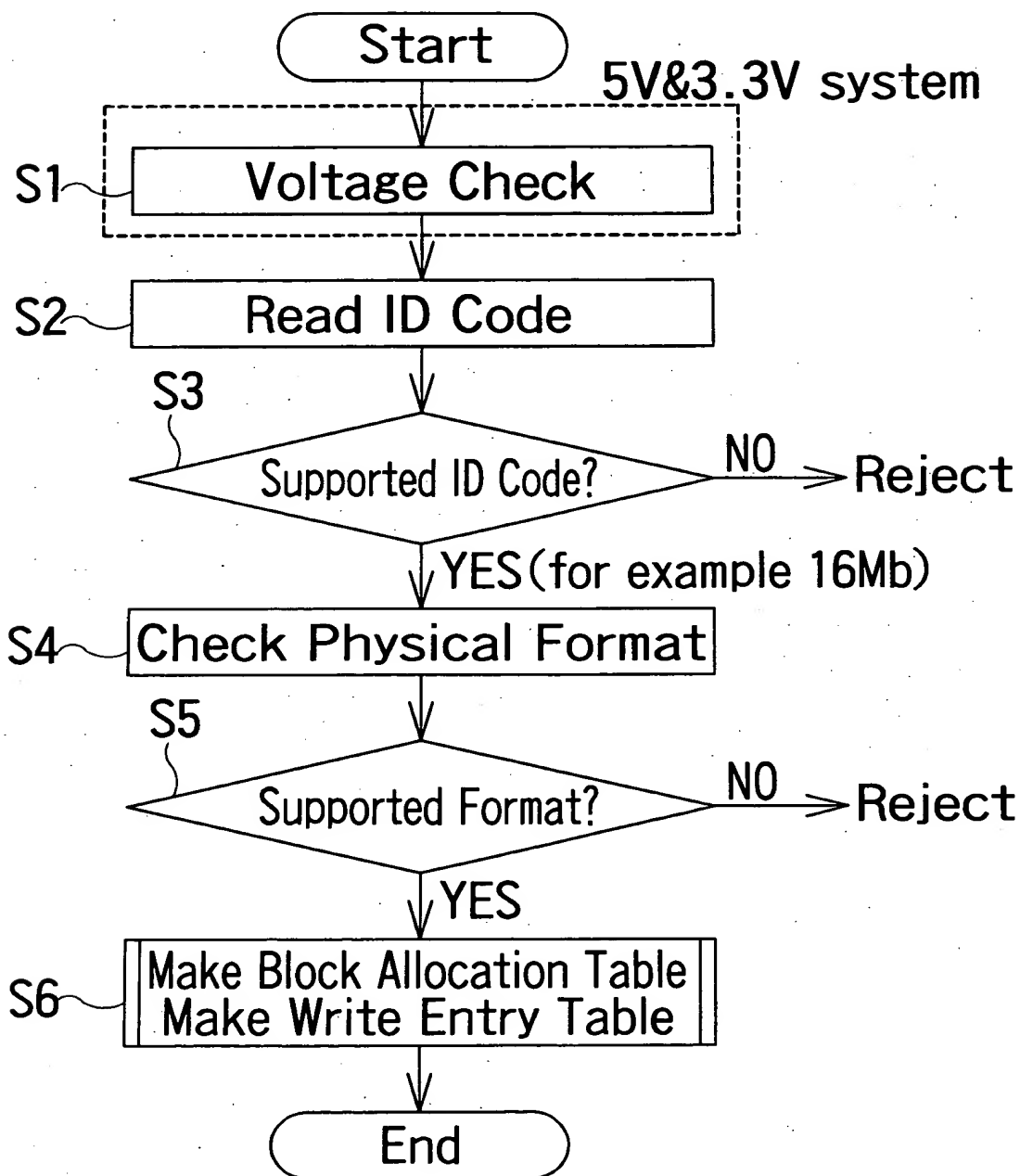


FIG. 32



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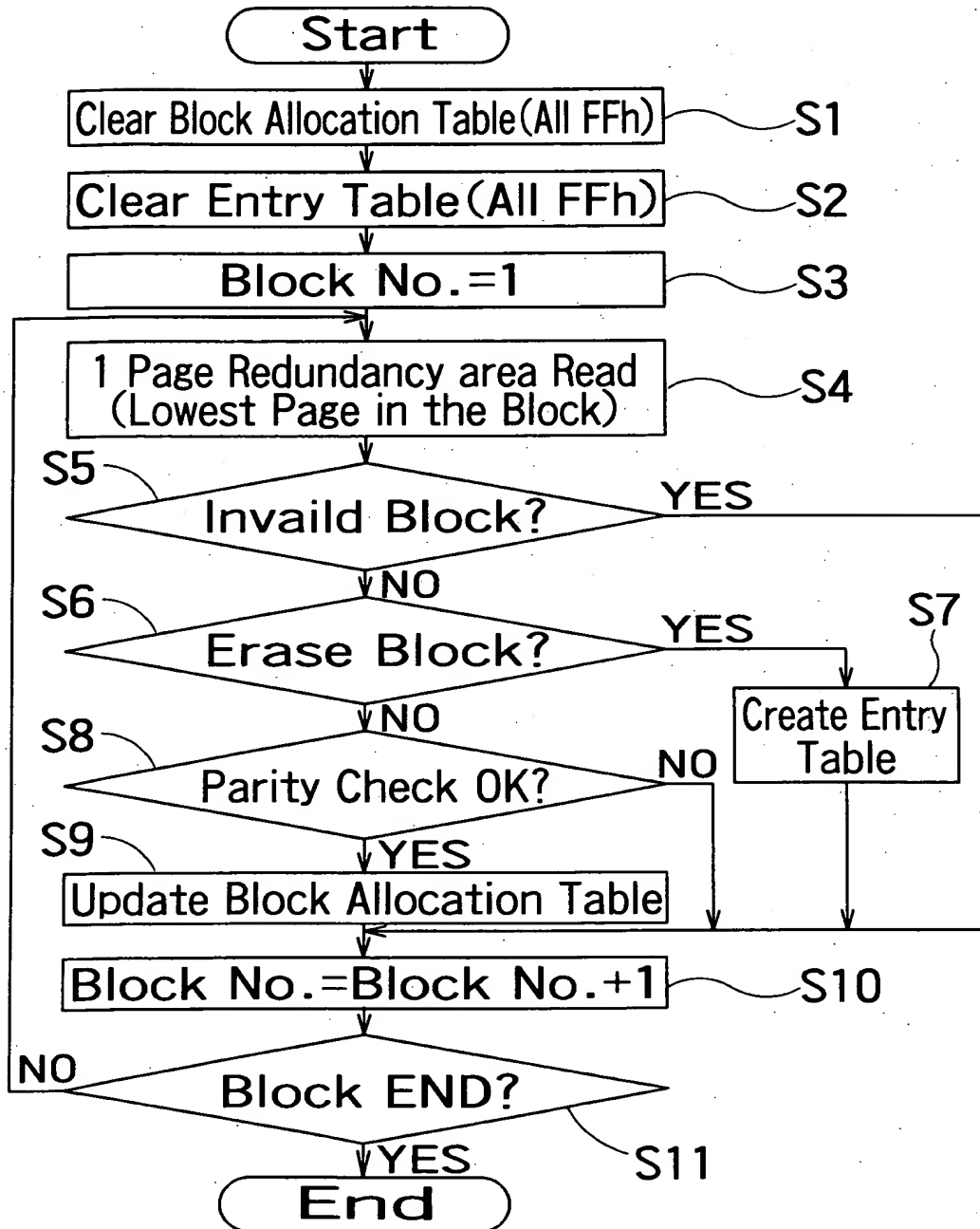


FIG. 33



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OFFSET (LOGICAL BLOCK ADDRESS)	PHYSICAL BLOCK AREA ADDRESS	PHYSICAL BLOCK AREA ADDRESS (BINARY DATA)	
Word0(LBA=0)	0	0000	0000
Word1(LBA=1)	250	1111	1010
Word2(LBA=2)	163	1010	0011
⋮	⋮	⋮	⋮
Word497(LBA=497)	122	0111	1010
Word498(LBA=498)	248	1010	1000
Word499(LBA=499)	64	0100	0000

1 PHYSICAL BLOCK AREA=2 PHYSICAL BLOCK

FIG.34



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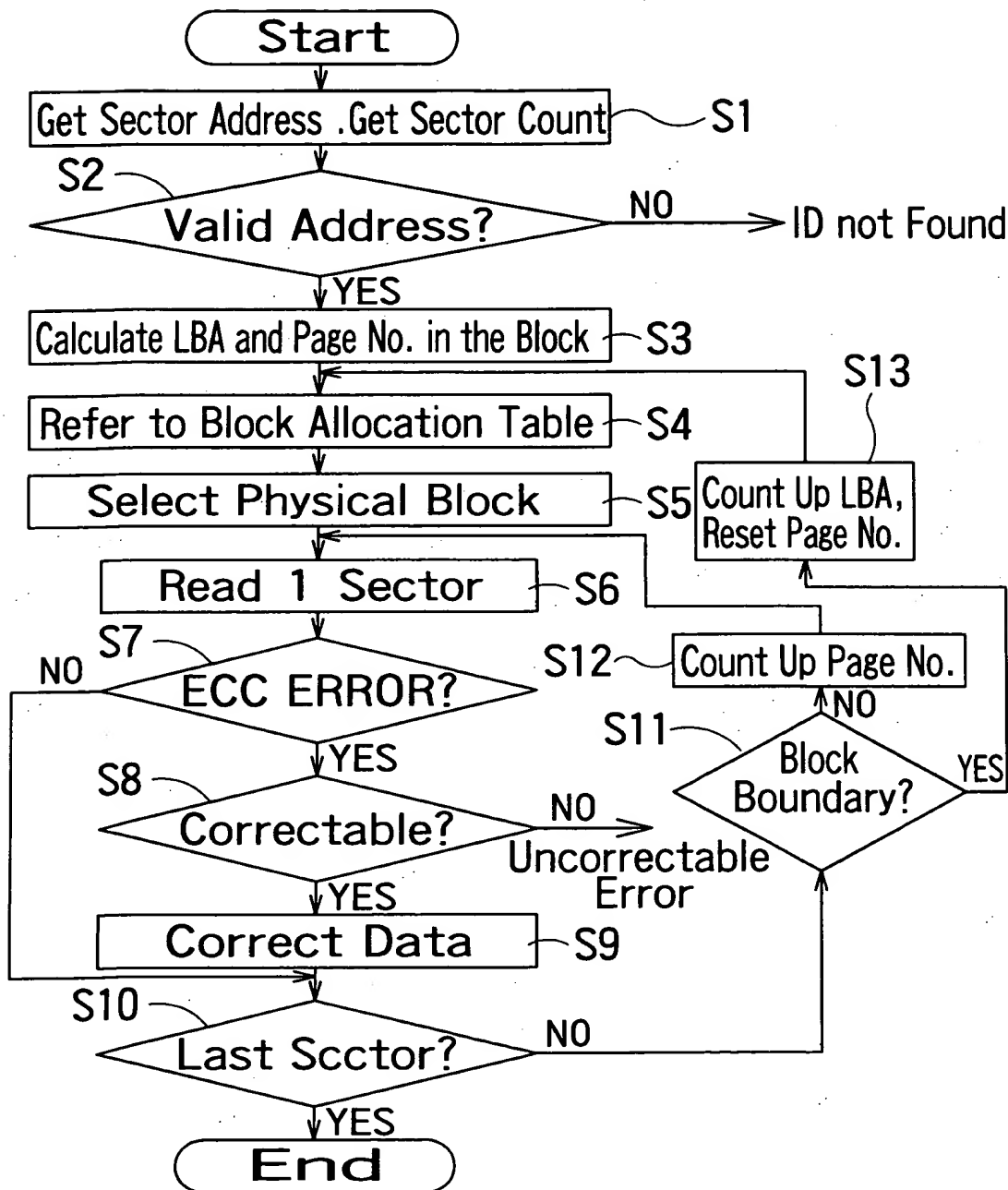


FIG. 35



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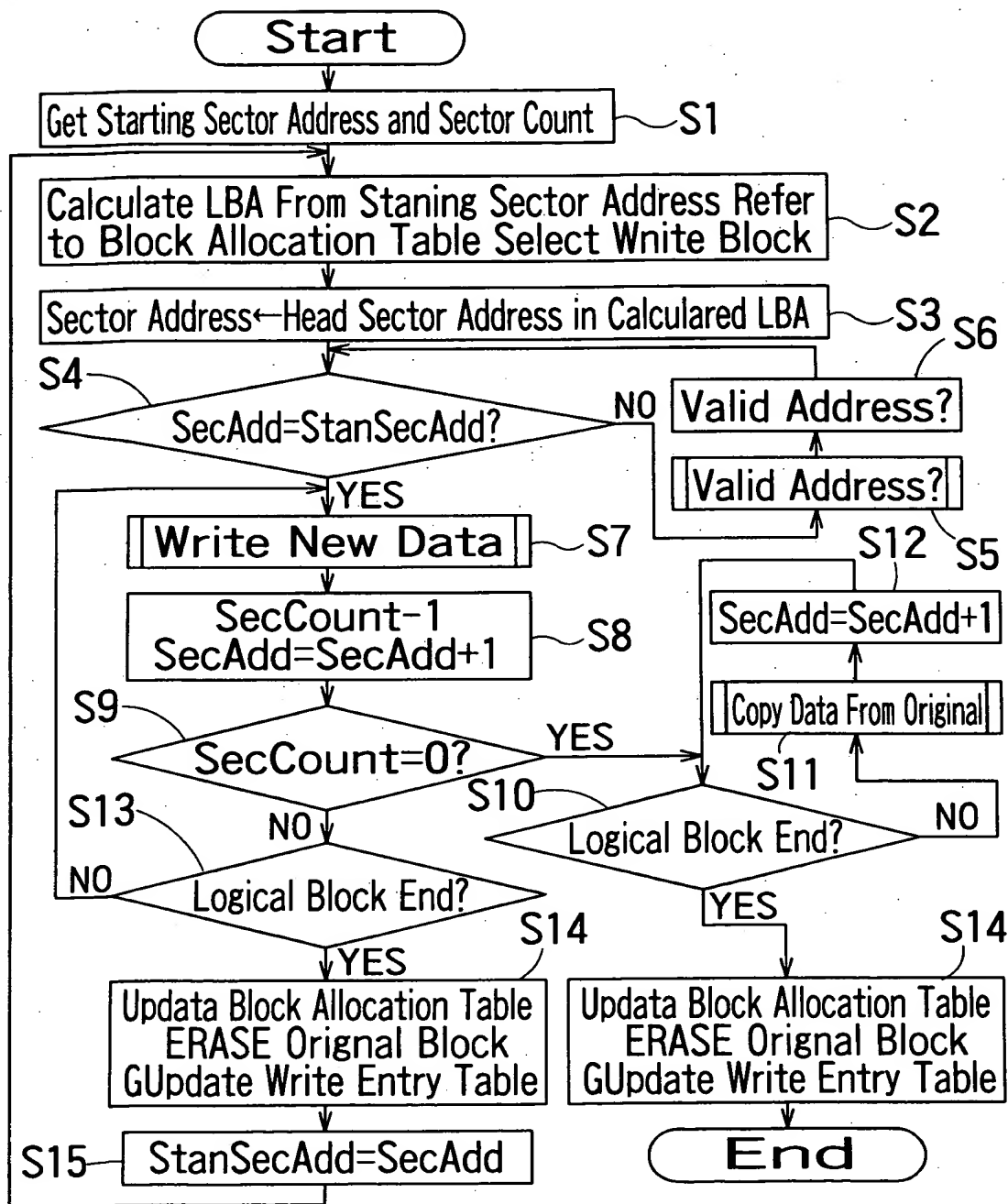
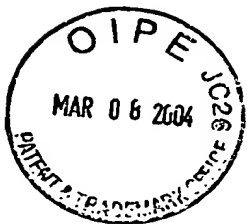


FIG. 36



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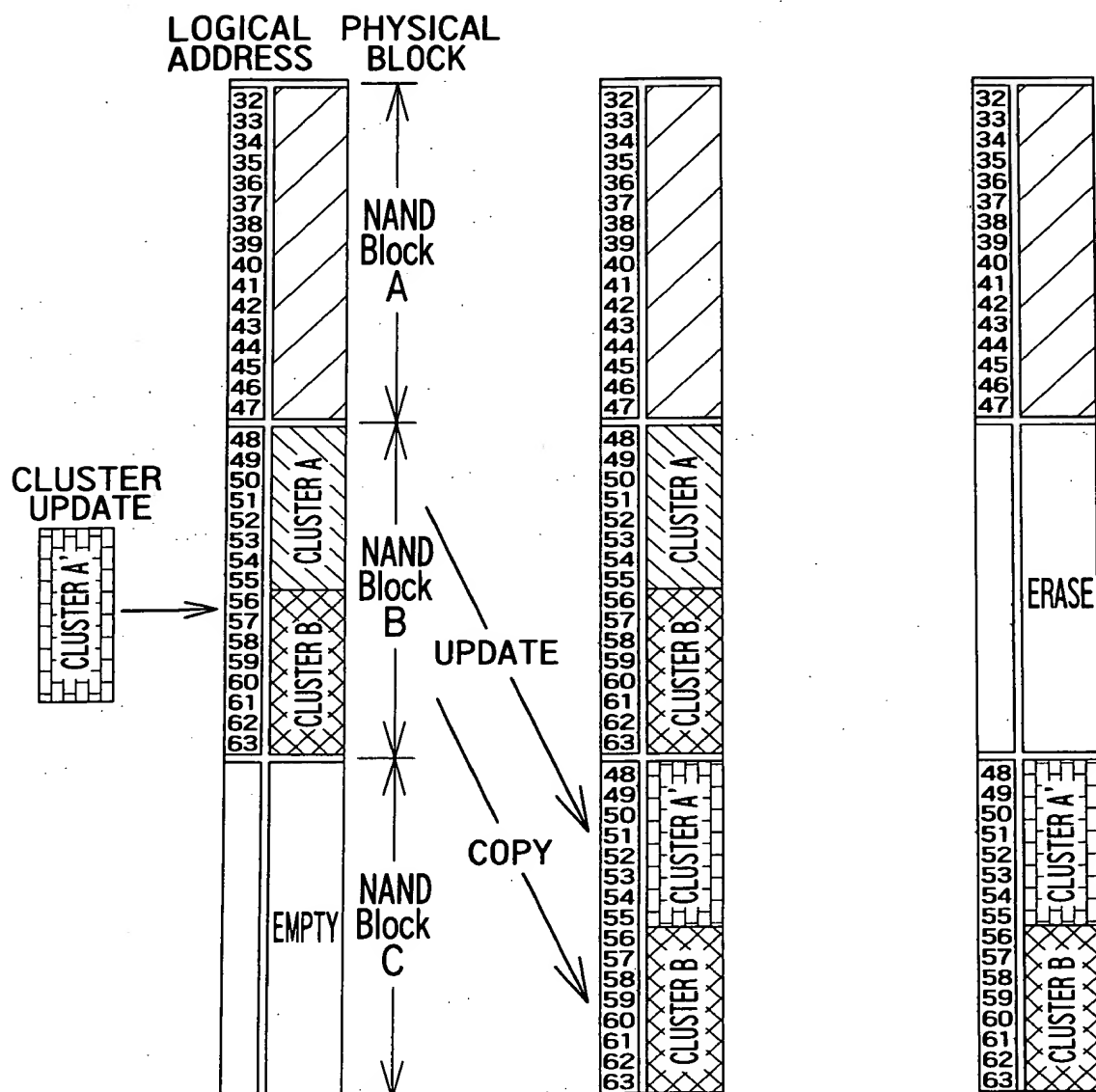


FIG. 38



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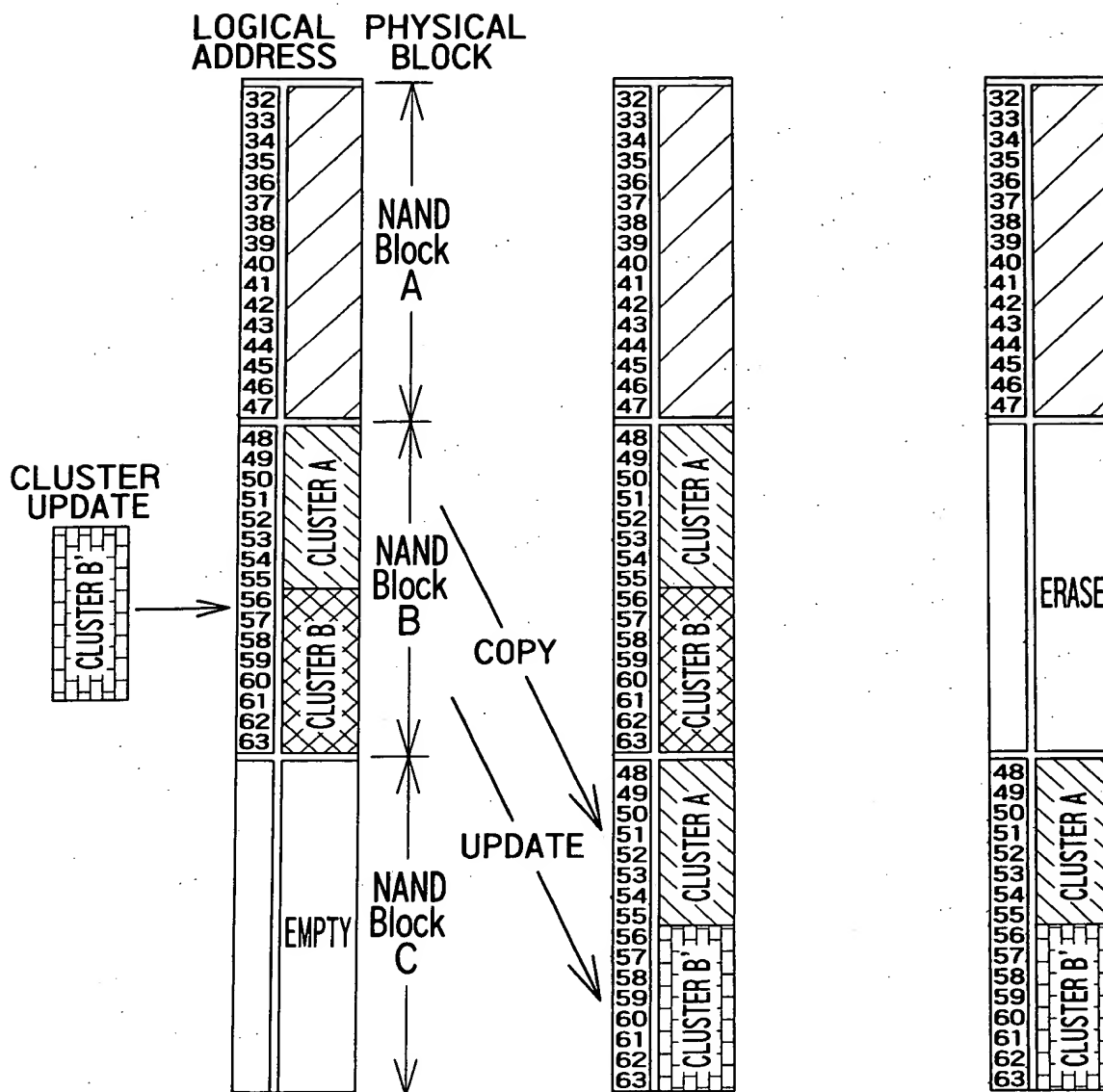


FIG. 39



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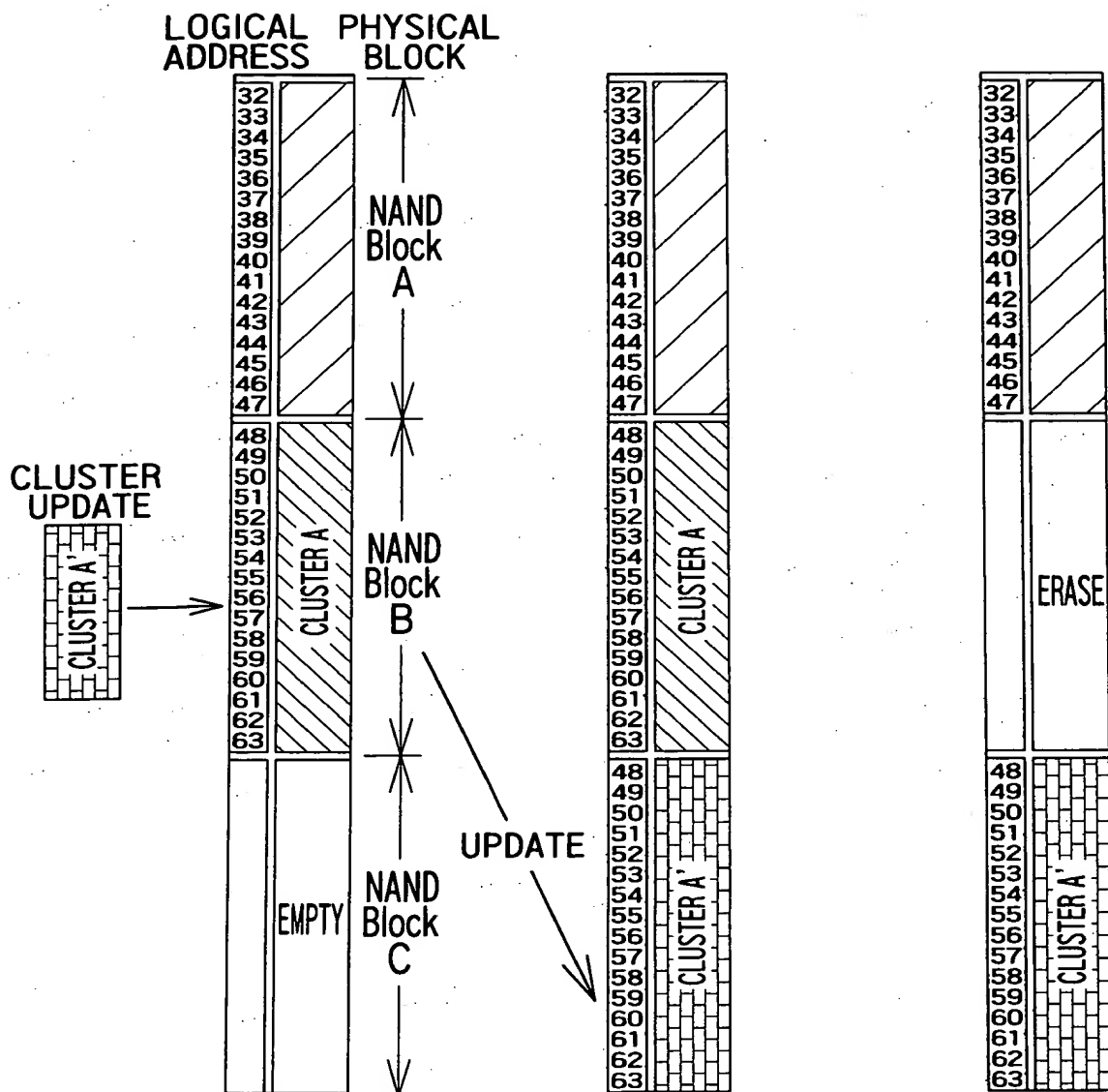


FIG. 40



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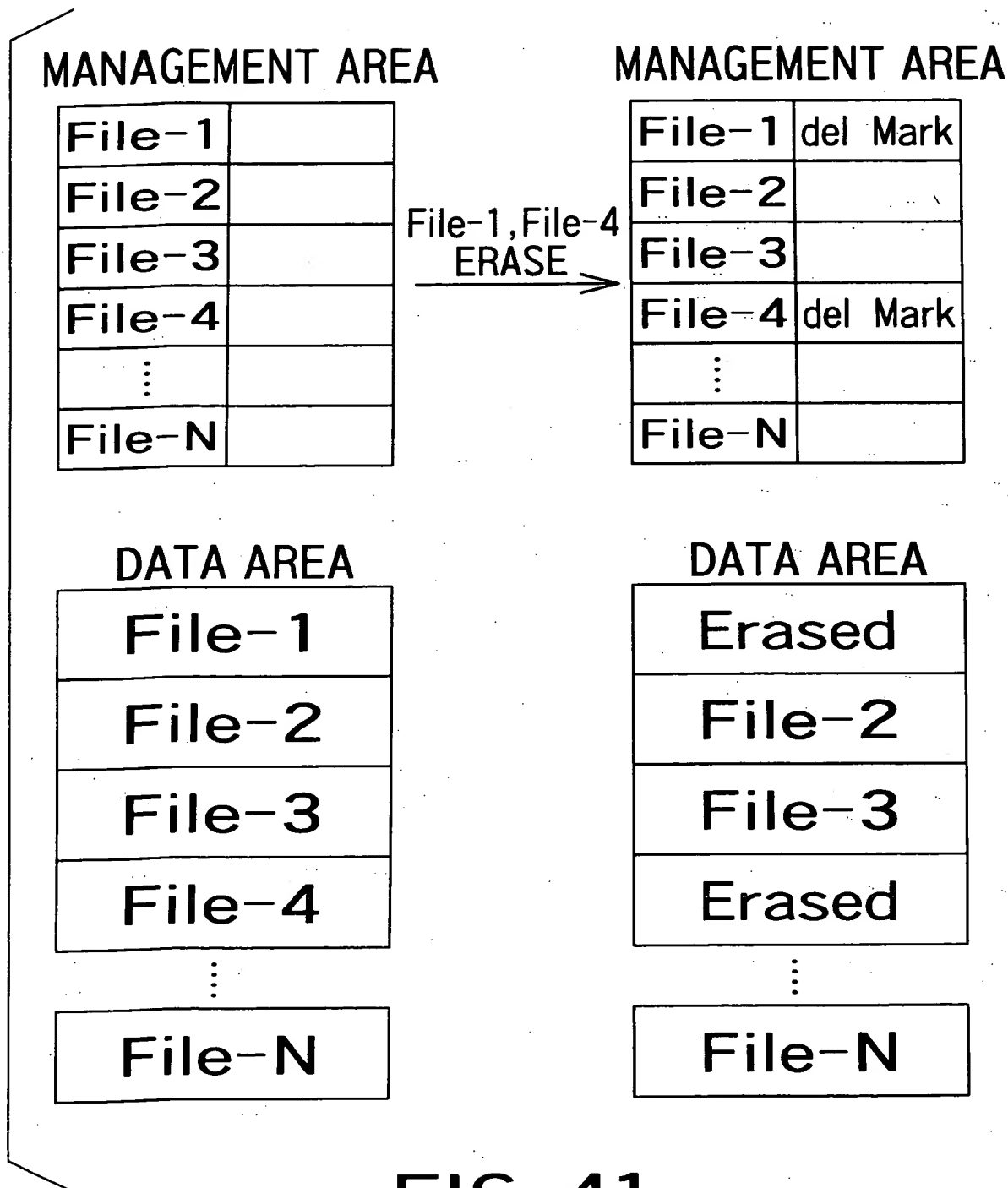


FIG. 41



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OFFSET (LOGICAL BLOCK ADDRESS)	(PHYSICAL BLOCK ADDRESS)	
	Upper Byte	Lower Byte
Word0 (LBA=0)	Physical Block Upper Address	Physical Block Lower Address
Word1 (LBA=1)	Physical Block Upper Address	Physical Block Lower Address
Word2 (LBA=2)	Physical Block Upper Address	Physical Block Lower Address
⋮		
Word247 (LBA=247)	Physical Block Upper Address	Physical Block Lower Address
Word248 (LBA=248)	Physical Block Upper Address	Physical Block Lower Address
Word249 (LBA=249)	Physical Block Upper Address	Physical Block Lower Address

FIG. 42(a)

OFFSET (LOGICAL BLOCK ADDRESS)	(PHYSICAL BLOCK ADDRESS)	
	Upper Byte	Lower Byte
Word0 (LBA=250)	Physical Block Upper Address	Physical Block Lower Address
Word1 (LBA=251)	Physical Block Upper Address	Physical Block Lower Address
Word2 (LBA=252)	Physical Block Upper Address	Physical Block Lower Address
⋮		
Word247 (LBA=497)	Physical Block Upper Address	Physical Block Lower Address
Word248 (LBA=498)	Physical Block Upper Address	Physical Block Lower Address
Word249 (LBA=499)	Physical Block Upper Address	Physical Block Lower Address

FIG. 42(b)



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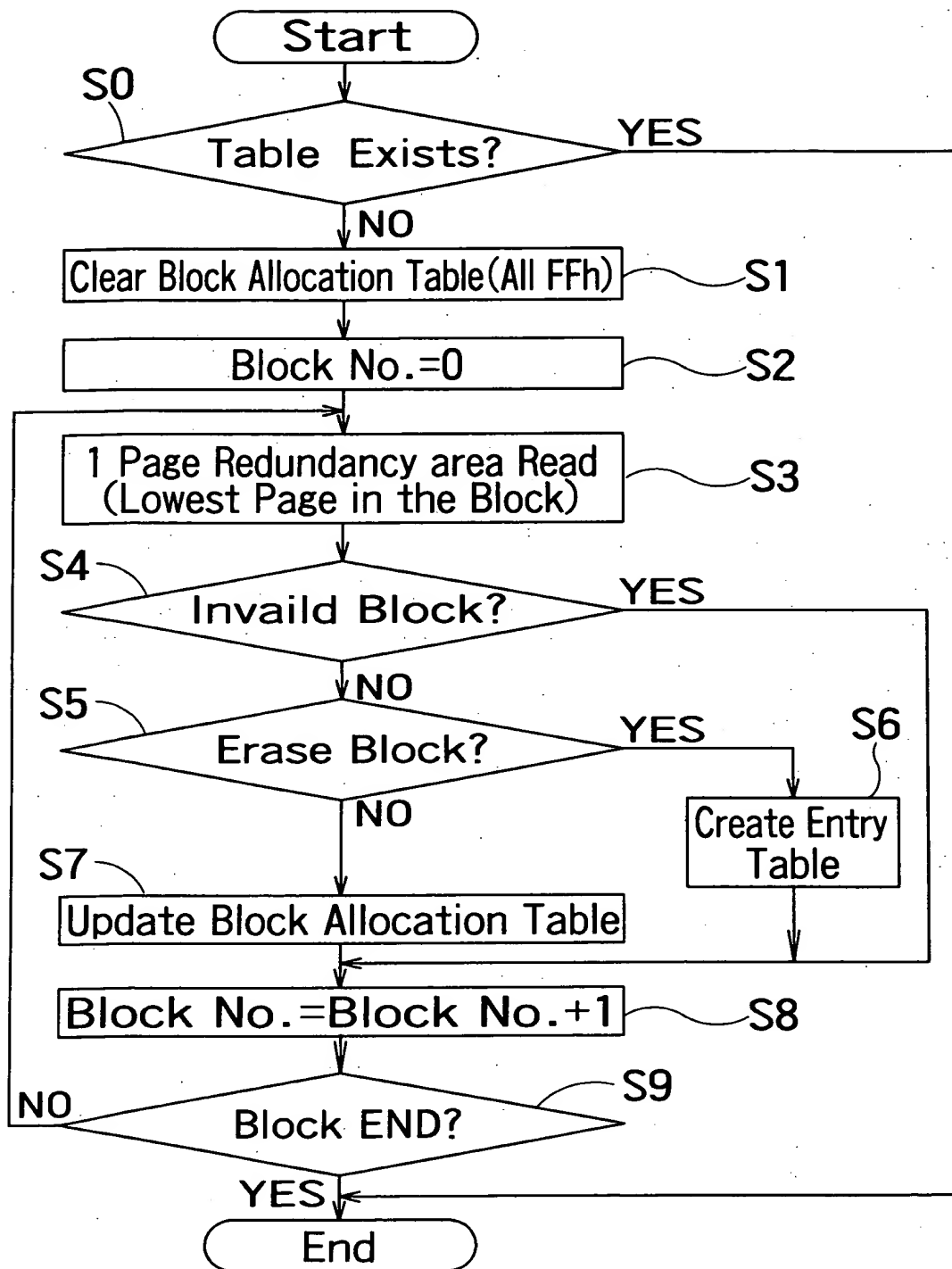
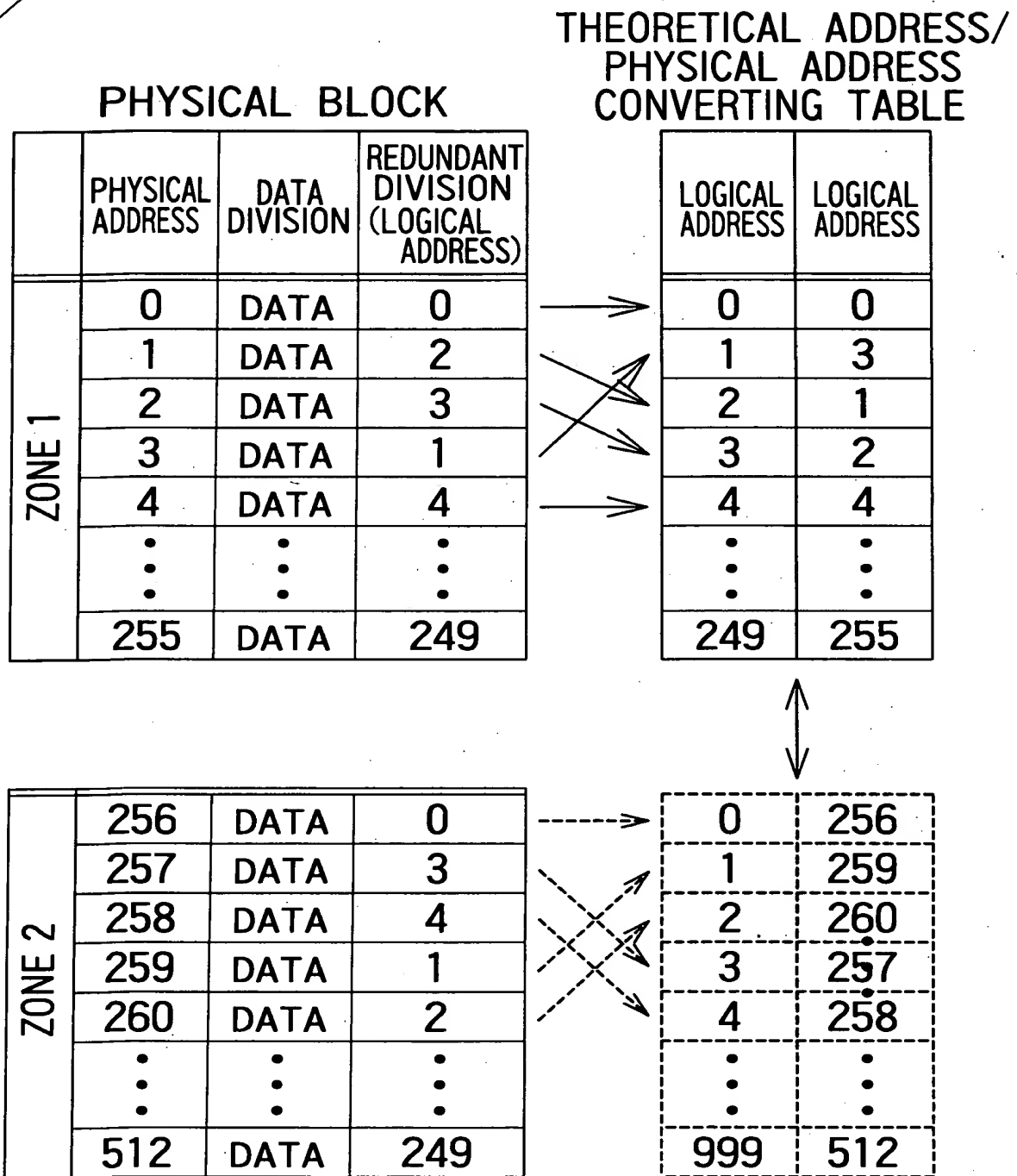


FIG. 43



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		OFFSET (LOGICAL BLOCK ADDRESS)	PHYSICAL BLOCK ADDRESS	PHYSICAL BLOCK ADDRESS (BINARY DATA)		
ZONE 1	Word0 (LBA=0)	0	0000	0000	0000	
	Word2 (LBA=2)	227	0000	1110	0011	
	⋮	⋮	⋮	⋮	⋮	
	Word254 (LBA=254)	244	0000	1111	0100	
	Word255 (LBA=255)	128	0000	1000	0111	
ZONE 2	Word256 (LBA=256)	256(256-256=0)	0000	0000	0000	
	Word257 (LBA=257)	327(327-256=71)	0000	0100	0111	
	⋮	⋮	⋮	⋮	⋮	
	Word499 (LBA=499)	500(500-256=244)	0000	1110	0000	
	Word500 (LBA=500)	428(428-256=172)	0000	1010	1100	

FIG. 45



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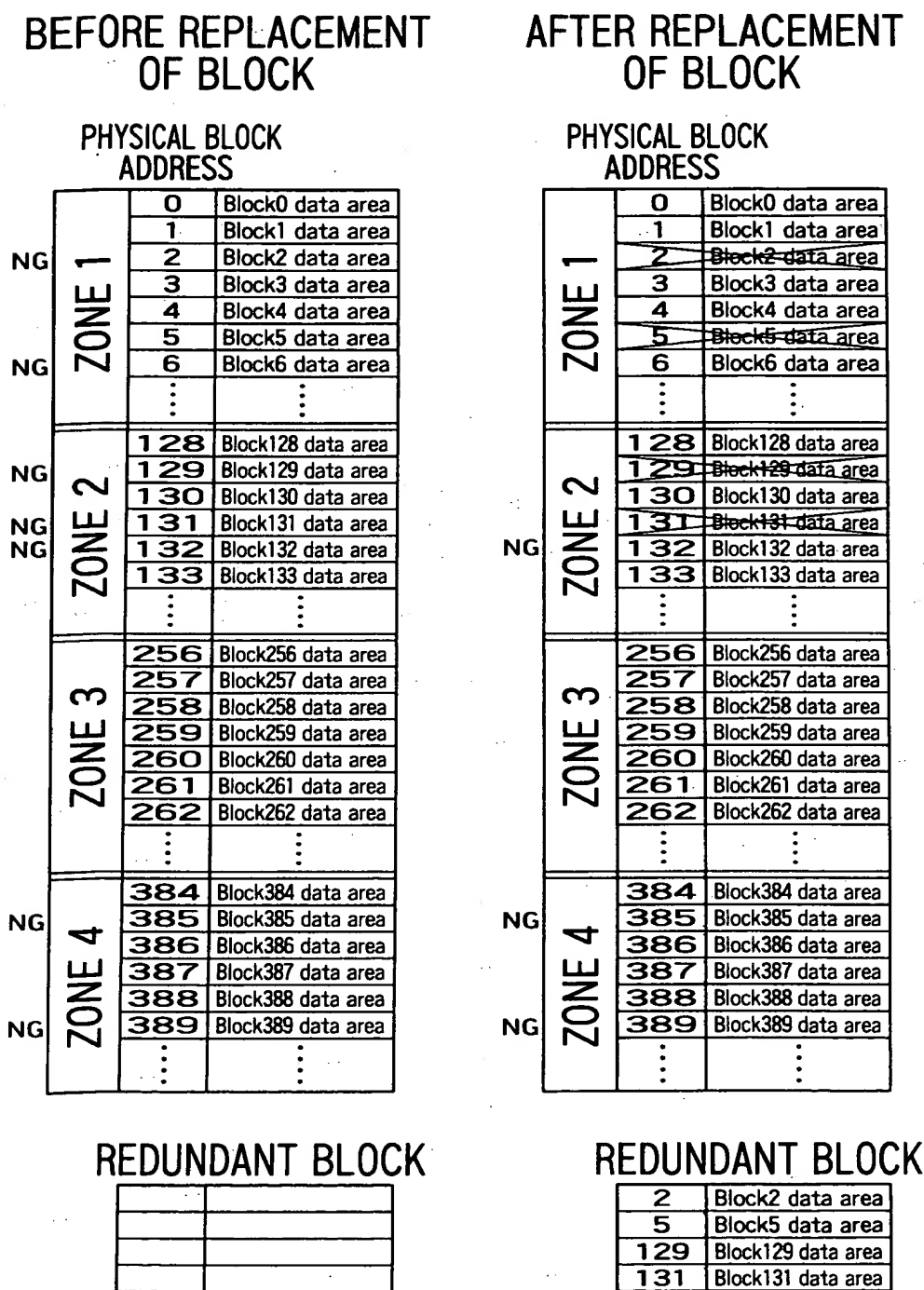


FIG. 46



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BEFORE REPLACEMENT
OF BLOCK

PHYSICAL BLOCK
ADDRESS

NG	0	Block0 data area
	1	Block1 data area
NG	2	Block2 data area
	3	Block3 data area
	4	Block4 data area
NG	5	Block5 data area
NG	6	Block6 data area
	7	Block7 data area
	8	Block8 data area
NG	9	Block9 data area
	10	Block10 data area
NG	11	Block11 data area
	12	Block12 data area
	13	Block13 data area
	14	Block14 data area
	⋮	⋮
NG	256	Block256 data area
	257	Block257 data area
	258	Block258 data area
NG	259	Block259 data area
	260	Block260 data area
NG	261	Block261 data area
	262	Block262 data area
	263	Block263 data area
NG	264	Block264 data area
NG	265	Block265 data area
	266	Block266 data area
	267	Block267 data area
	268	Block268 data area
NG	269	Block269 data area
	⋮	⋮

REDUNDANT BLOCK

AFTER REPLACEMENT
OF BLOCK

PHYSICAL BLOCK
ADDRESS

	0	Block0 data area
	1	Block1 data area
	2	Block2 data area
	3	Block3 data area
	4	Block4 data area
	5	Block5 data area
	6	Block6 data area
	7	Block7 data area
	8	Block8 data area
	9	Block9 data area
	10	Block10 data area
	11	Block11 data area
	12	Block12 data area
	13	Block13 data area
	14	Block14 data area
	⋮	⋮
NG	256	Block256 data area
	257	Block257 data area
	258	Block258 data area
NG	259	Block259 data area
	260	Block260 data area
NG	261	Block261 data area
	262	Block262 data area
	263	Block263 data area
NG	264	Block264 data area
NG	265	Block265 data area
	266	Block266 data area
	267	Block267 data area
	268	Block268 data area
NG	269	Block269 data area
	⋮	⋮

REDUNDANT BLOCK ^ HARDWARE REDUNDANT

REDUNDANT BLOCK ^ HARDWARE REDUNDANT

REDUNDANT BLOCK ^ HARDWARE REDUNDANT

REDUNDANT BLOCK ^ HARDWARE REDUNDANT

REDUNDANT BLOCK ^ HARDWARE REDUNDANT

REDUNDANT BLOCK

0	Block0 data area
2	Block2 data area
4	Block4 data area
5	Block5 data area
9	Block9 data area
11	Block11 data area

FIG. 47



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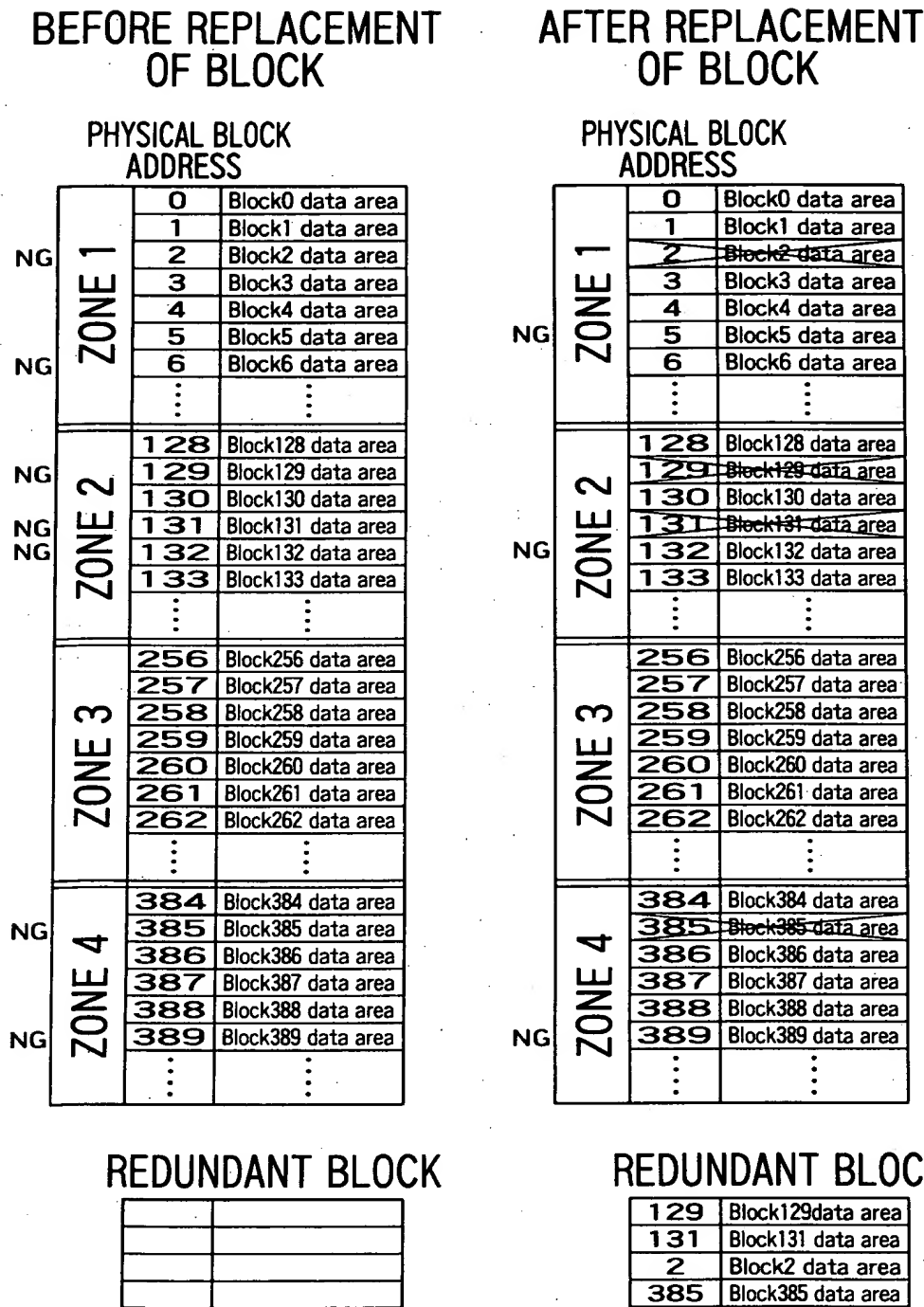


FIG. 48



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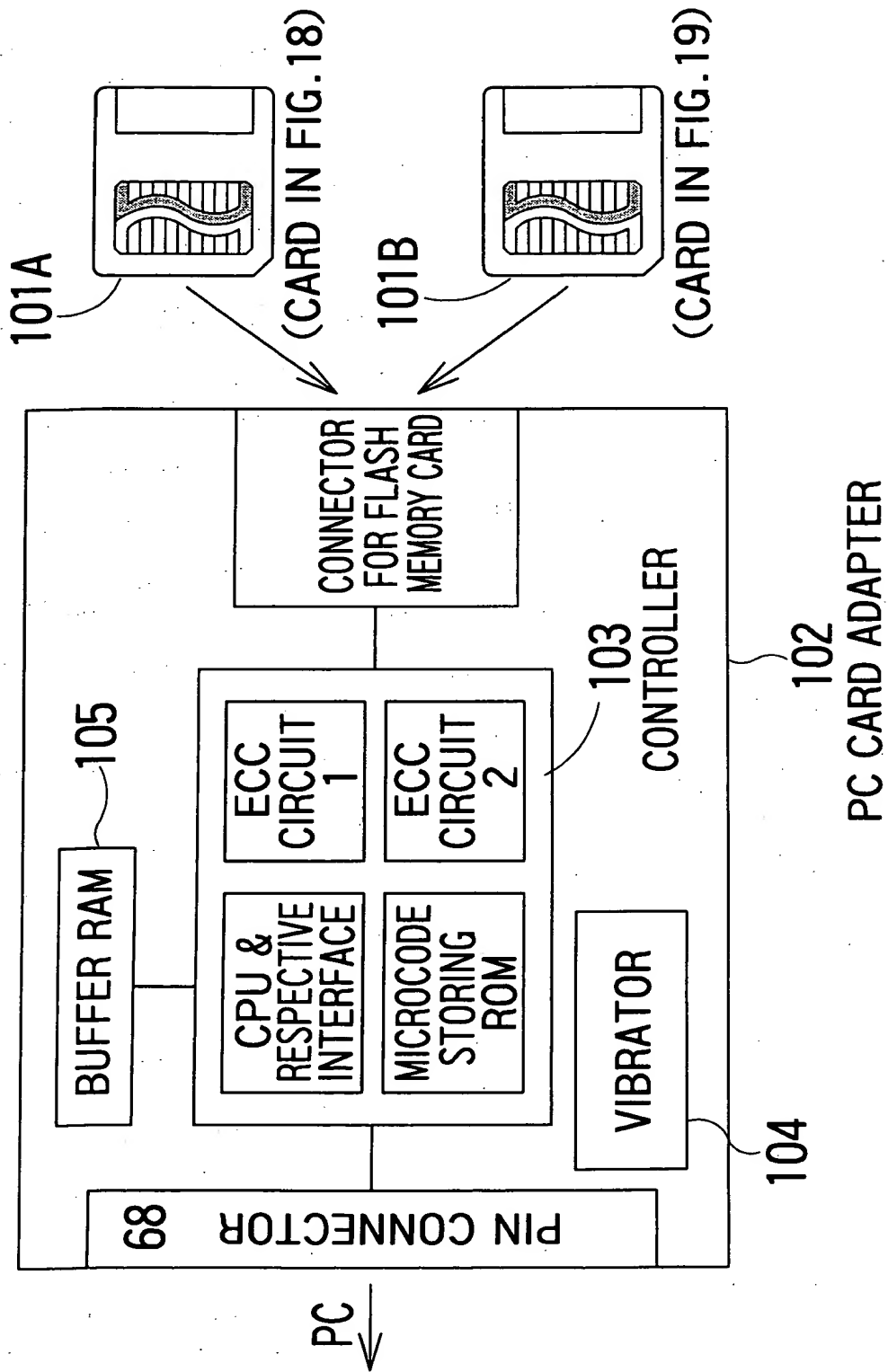


FIG. 49



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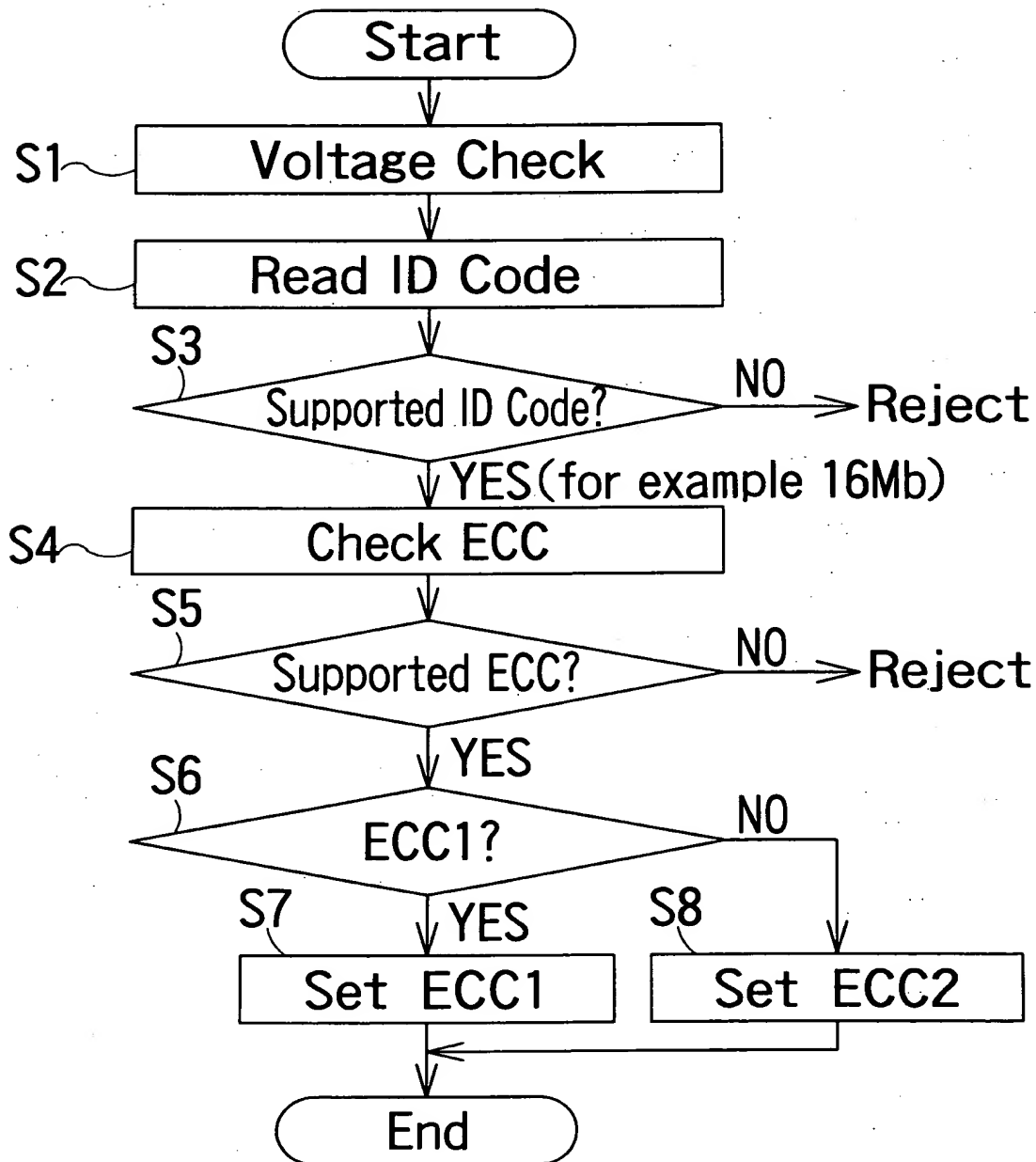


FIG. 50



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DATA DIVISION

BYTE	PAGE 0(EVEN PAGE)	PAGE 1(ODD PAGE)
0~255	DATA Area-1	DATA Area-2

REDUNDANT DIVISION

BYTE	EVEN PAGE	ODD PAGE
256	ECC Flag Area	ECC Area-2
257	ECC Area-3	
258		
259		
260	Data Status Area	Block Address Area-2
261	Block Status Area	ECC Area-1
262	Block Address Area-1	
263		

FIG. 51



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	ECC-AREA1	ECC-AREA2	ECC-AREA3	ECC-AREA4
ECC METHOD 1	ECC CODE FOR DATA AREA-1	ECC CODE FOR DATA AREA-2	NULL (ALL "FFh")	ECC1-FLAG
ECC METHOD 2	ECC CODE FOR DATA AREA-1,2	ECC CODE FOR DATA AREA-1,2	ECC CODE FOR DATA AREA-1,2	ECC2-FLAG

FIG. 52